JS 26
INTELLIGENT TOOLS AND METHODS FOR RADIO SCIENCE

Embedded optimization of 90° Hybrid couplers in 4 chips power combined frequency doublers at 345GHz

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Abstract

The generation of strong continuous wave sources at submillimetre wavelength and Terahertz frequencies for the implementation of local oscillator source remains a challenge in terms of output power. Solid-state sources often feature cascaded frequency multiplier stage that are at their maximum power rating. New robust architectures have to be developed, to increase the power handling and distribute evenly the power over several diodes. Power combined frequency multipliers at submillimetre wavelength feature two or more chips in parallel combined at their input / output ports with Y or hybrid junction elements. Each element of the structure is often optimized separately, assuming an ideally matched impedance at their waveguide interface. We investigate the embedded optimization of 90° hybrid couplers to minimize phase and amplitude imbalance at the input of frequency multiplier elements, while keeping impedance matching across frequencies.

1 Introduction

Spectral analysis of the planets' atmospheric content in the submillimetre frequency range is performed by heterodyne instruments in order to reach a spectral resolution of 10^7 or better. The detection can be conducted by semiconductors (Schottky mixers), with local oscillator (LO) sources which requires the signal power to be of the order of the milliwatts. Compact Terahertz LO sources in space systems are typically composed of an oscillator, power amplifiers (PAs) and frequency multiplier stages [1]. The LO chain output power is limited by the frequency multiplier efficiency and the PA output power. One of the major difficulties is the power handling of the diodes at the earliest stage right after the PA. In fact, the multiplier stages are at their maximum power rating. In this study, we discuss the development of ultra balanced high output power sources based on frequency multiplication and power combining scheme to generate LO sources at Terahertz frequency. In particular, we focus on the distribution of the signal through multiple criteria: amplitude, phase imbalance at chip level and even distribution of the coupled power at diode level. We first explain the functioning of power combined architectures in part 2, then we present a novel method to improve the balance in power combined multiplier design in part 3. Finally, we develop and compare two power combined frequency doublers architectures at 300 GHz (as reference) and 345 GHz (novel optimization) in part 4. In this study we use the 300 GHz frequency doubler from the SWI instrument of the JUICE mission. This frequency doubler reaches 20% of efficiency in both single (D300X1) and dual chip (D300X2) configuration, similarly to other state-of-the art doublers [2-6].

2 Power combined architecture (PCA) and problematics

The power combining technic consists in splitting a signal with a 90°phase shift (in the case of a frequency doubler) or in phase (in the case of a tripler) and recombine it at the output. In the particular case of the PCA with doublers considered here, a hybrid coupler and a Y-junction [5] are used respectively at the input and output ports. To extend to a greater number of chips, we can add several 90° hybrid couplers and Y-junctions and the input and output respectively, as illustrated in figure 1, that represents a case of a four chips power combined doubler structure. Consequently, in order to increase input power of a multiplier, we can duplicate those chips to double, quadruple etc. the acceptable input power.

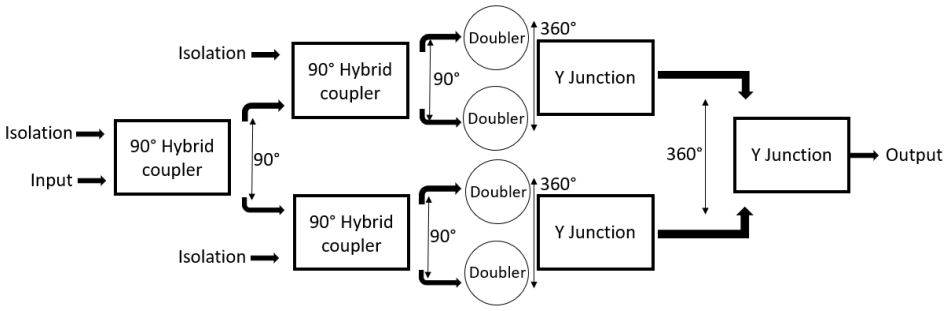

Figure 1. Diagram of 4-chip power combining design. Elements and corresponding phase differences at each stage are shown in degrees.

However, implementing this technic to a larger number of chips has its limitations. First, phase losses grow with imbalance and cascade of couplers. Therefore, a control of the phase imbalance is crucial for higher orders of power combinations. Above 20°, the loss starts to be visible but not discriminant, above 28° the loss becomes more significant (-1dB) and from 45° the power combining is no longer beneficial. These values are calculated for the worst case of a cascade of couplers with the same phase imbalance value. See figure 2.

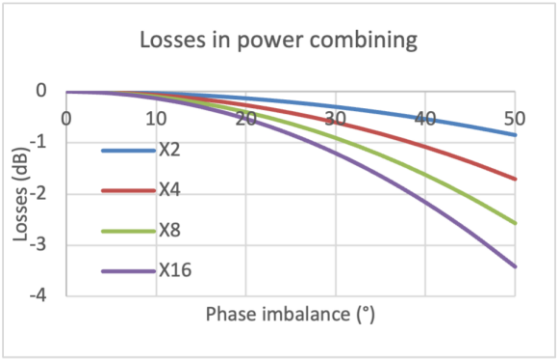

Figure 2. Losses of a recombined signal as a function of phase imbalance. X2, X4, X8 and X16 curves corresponds to cases of 2, 4, 8 and 16 chips power combining architectures. Values calculated for worst case where all the recombining elements have the same phase imbalance.

Secondly, we have to consider the power handling limit of each chips [7], in order to provide a secure environment of operation without damaging the chip. We need to control how well the power is distributed among the chips (and its diodes) and, therefore, limit uneven diodes ageing between chips. A first solution is to use derating techniques [8] to keep the power acceptable and space qualified limits [7], but this is at the cost of performance and efficiency. A second solution considered here is to analyse the imbalances of the structures and how to correct it.

3 Methodology for the design of balanced PCAs or embedded hybrid optimization method

To simulate the frequency multipliers in power combined architectures, we use a co-simulation technique. The electromagnetic simulation (EM) is performed using Ansys HFSS to generate two scattering parameters files, respectively for the fundamental and second harmonic signals. These files are then fed to the electric harmonic balance simulation [9] using Keysight ADS. It is very often that each element (multiplier, hybrid or Y-junction) is designed separately with waveguide interfaces. In this case, the 4-port 90° hybrid coupler is designed in the way to present nominal waveguide characteristic impedance at each port. Even if the designer might have freedom to choose the amplitude and phase imbalance of the coupler [10], [11], the input impedance of the chips -thus the impedance that will be seen by the coupler- can deviate significantly from the waveguide characteristic impedance. Indeed, depending on the impedance seen by one chip, the input impedance of its "twin" can be different. In addition, the input impedance of one chip itself is highly dependent on the input power and bias levels. These three factors impact directly the amplitude and phase imbalance value of the coupler. For this reason, we have developed a coupler model with lumped elements that is optimizable in the electric schematic of the full power combined architecture. This co-optimized electrical element allows to optimize for the most suitable impedance, the best amplitude and phase imbalance to strengthen power-combined frequency doubler architectures.

The lumped element model of the hybrid coupler uses a combination between Marcuwitz's Tee lumped model [12] and Keysight ADS' Rectangular Waveguide model. This coupler model is embedded directly in the optimization setup of the whole power combined doubler. Physical lengths of the coupler are optimized values, and the analytical values of the lumped components are calculated from it, as illustrated in figure 3. After co-optimization, a 3D electromagnetic model of the hybrid coupler is generated using the resulting lengths. In order to minimize possible discrepancies between the performances of the EM and the lumped model, we use the space mapping technique [13]: the lumped model is re-optimized to target the difference of the performances. And the differences of physical dimensions are subtracted in the EM model.

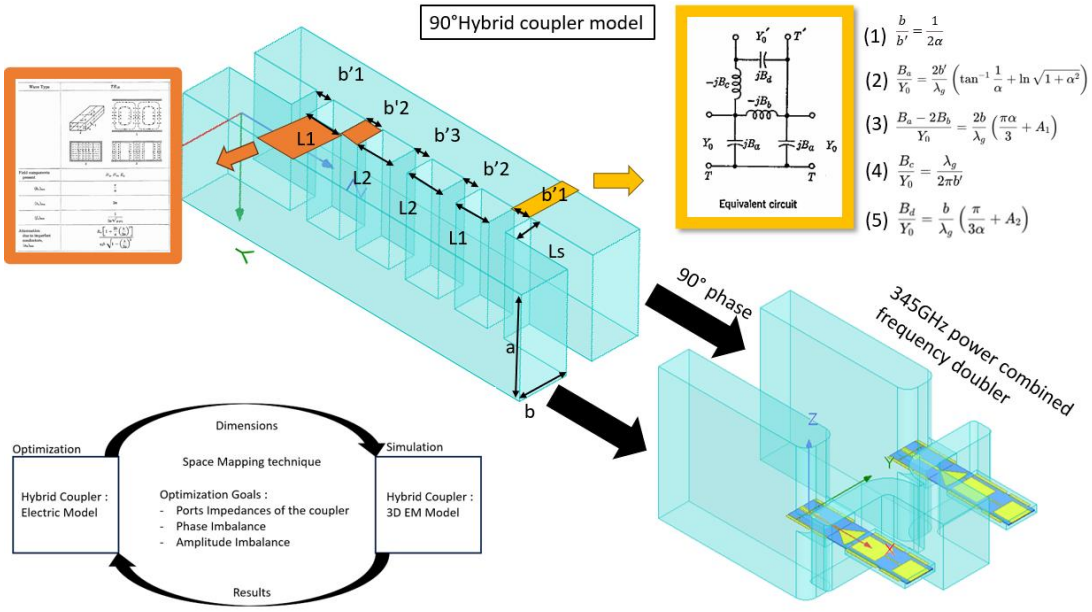

Figure 3. Top: Diagram of the optimization with lumped model of 90° hybrid coupler. Bottom: space mapping [13] optimization diagram.

4 Application on 300 and 345 GHz power combined frequency doublers.

In order to test our methodology, we designed two different prototypes: first, we set up a sequence of reference designs: a single chip 300 GHz doubler (D300X1), a 2-chips PCA 300 GHz doubler (D300X2) and a 4-chips PCA 300 GHz doubler (D300X4), with every element (Hybrid, Y-junction and chips) designed separately, and secondly, we use the "embedded hybrid optimization method" to develop a 2-chips PCA 345 GHz doubler (D345X2) and a 4-chips PCA 345 GHz doubler (D345X4).

In the first prototype, all stages were optimized separately to a standard rectangular waveguide characteristic impedance. These new designs are replicated two times for the D300X2 [8] and connected with the same 90° Hybrid Coupler input and Y-junction output.

In the second prototype 345GHz doublers were designed by scaling the 300GHz doubler to shift its centre frequency to meet the requirements of [14]. From this new design, two separated sequences of D345X2 and D345X4 are generated using the "embedded hybrid optimization method". The Y-junction remains identical for all devices. The hybrid coupler (stage X4 of figure 4) feeding the two D345X2 that forms the D345X4 is also optimized with Part 3 methodology.

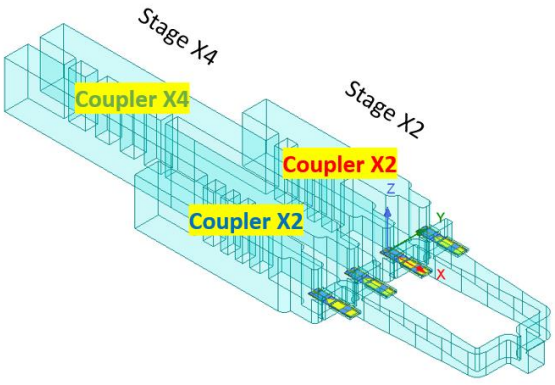

Figure 4. 3D screenshot of the EM model of the D345X4 developed using the "embedded hybrid optimization method" described in part 3. The D300X4 has the same architecture.

We compare in figure 5 the amplitude and phase imbalance at the level of every coupler constituting the D300X4 (dashed lines) and D345X4 (plain lines) architectures. Red and blue curve illustrate the amplitude and phase imbalance of the couplers at the X2 stage of figure 4. Green curve illustrates the amplitude and phase imbalance of the coupler at the X4 stage of figure 4. We see that the amplitude imbalance is reduced from 6dB to less than 2dB over the operation bandwidth for the two couplers of the X2 stage. In addition, the phase imbalance is reduced from 30° to less than 10° of deviation from 90° over the operation bandwidth. We also notice from the green curves that most of the imbalance is corrected from the first stage of couplers (stage X2) that are directly facing the chips. The first stage of impedance matching is the most sensible [15]. We can see in figure 6, that despite the compensation of the proposed method, some imbalance persists at the diode scale within a same chip. When designing ultra-balanced frequency multipliers, this unbalance between multiplier branches of diodes or diodes of a same branch is a problem that needs to be to addressed directly on the chips' transmissions lines and that cannot be compensated by the combining elements only.

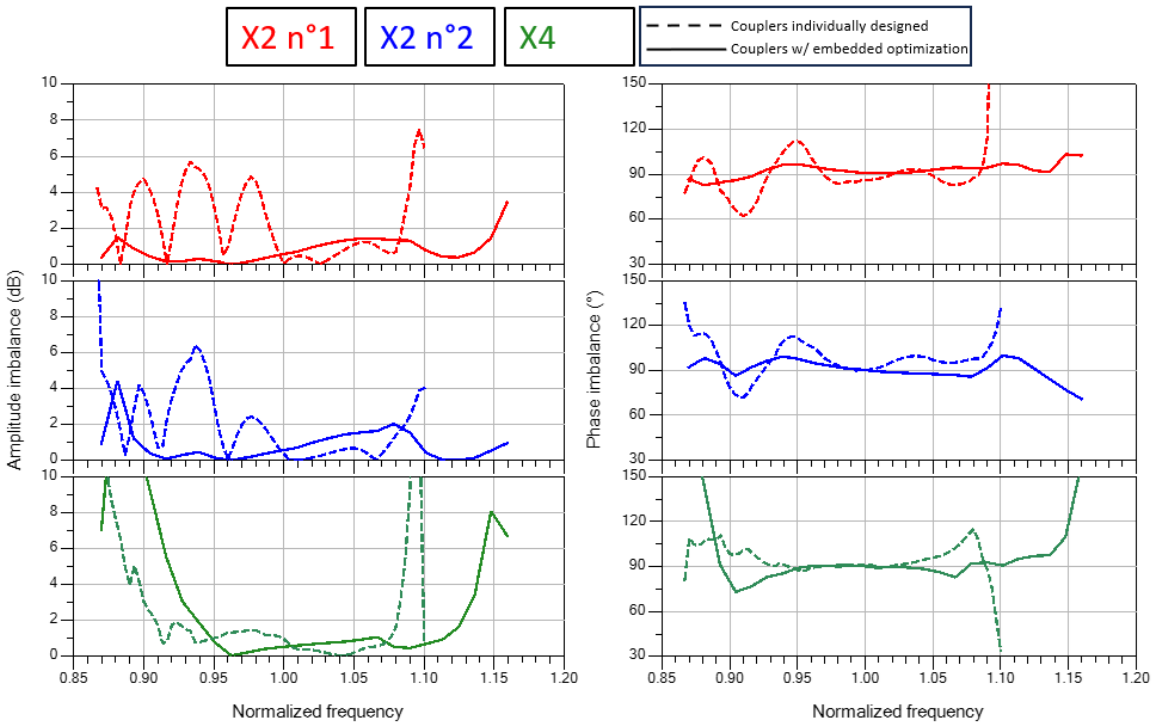

Figure 5. Amplitude imbalance (left) and phase imbalance (right) at the output of each hybrid couplers of the D300X4 (dashed lines) and D345X4(plain lines) architectures. Red and blue curve illustrate the amplitude and phase imbalance of the couplers at the X2 stage of Figure 4. Green curve illustrates the amplitude and phase imbalance of the coupler at the X4 stage of Figure 4. The x-axis is displayed in normalized frequency to allow comparison of the 300 and 345 GHz doublers.

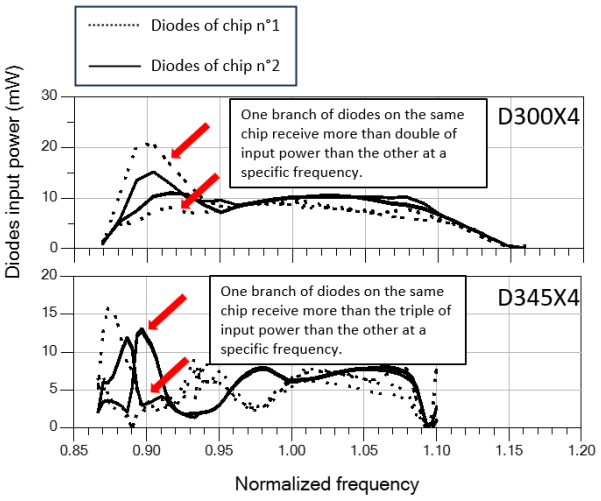

Figure 6. Left: Input power received by each diode. Diodes on the same chip are traced with the same type of line. Top: D300X2 diodes. Bottom: D345X2 diodes.

The amplitude imbalance for all three couplers of the D300X4 is improved (lowered) with higher input power. Indeed, an increased in the input power flattens the input impedance per chip around a resistive and reactance value. This led to an improvement of the impedance matching, thus a reduction of the amplitude and phase imbalance in existing designs. However, this improvement needs to be confirmed, if the current is not kept within the limit of the current velocity saturation value defined in [16]. In this case, the displacement current flowing through the diode increases with input

power, that results in an increase of the resistance. This effect (and exact expected resistance value) is not included in our simulation model, as we keep the current below the levels defined in [16].

Conclusion

We present an embedded hybrid optimization method for the development of power combined frequency doublers at submillimetre wavelength. We illustrate it with the results of a simulation of embedded optimization of 90° hybrid couplers for a four-chip power combined 345 GHz frequency doubler. We demonstrate improved amplitude and phase imbalances values when compared to a reference 300 GHz four-chip frequency doubler architecture using 90° hybrid coupler individually designed. The simulations will be validated by measurements in the near future. The 4-chip 345 GHz doubler manufacturing deviation will be evaluated. A fabricated version of this doubler will have one DC-port per chip, in order to monitor the solicitation's balance of each chip.

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